**Lab 03**

**Implementation of a 8 bit Ring Counter**



Spring 2025

CSE-308L

Digital System Design Lab

Submitted by: Naveed Ahmad

Registration No.: 22PWCSE2165

Class Section: B

Student Signature: \_\_\_\_\_\_\_\_\_\_\_\_\_\_

Submitted to:

Engr. Shah Zada Fahim Jan

05 April 2025

Department of Computer Systems Engineering

University of Engineering and Technology, Peshawar

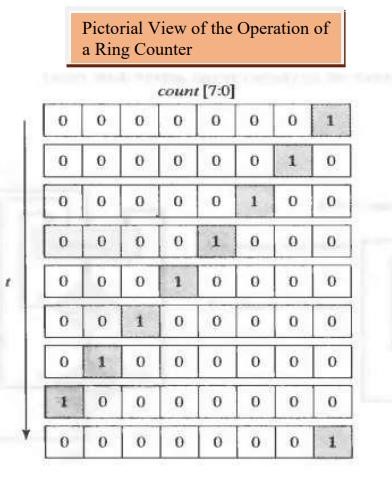
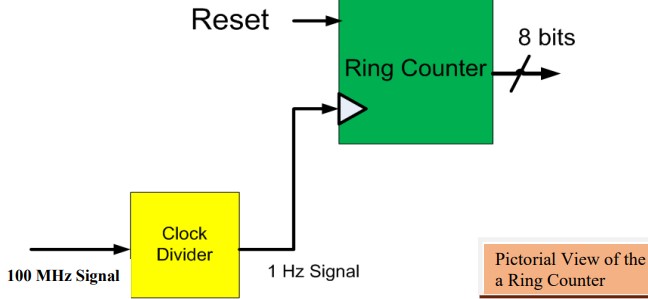
**LAB 06:**

**Implementation of a 8 bit Ring Counter**

OBJECTIVE:

* To become familiarized with behavior level modeling
* To be able to implement sequential circuits using Verilog
* To Implement an 8 Bit Ring Counter on Spartan 6 FPGA starter kit

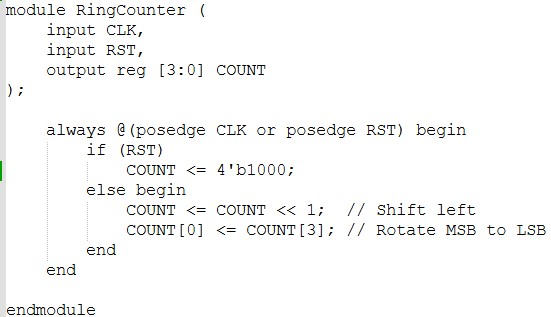
**Block Diagram:**



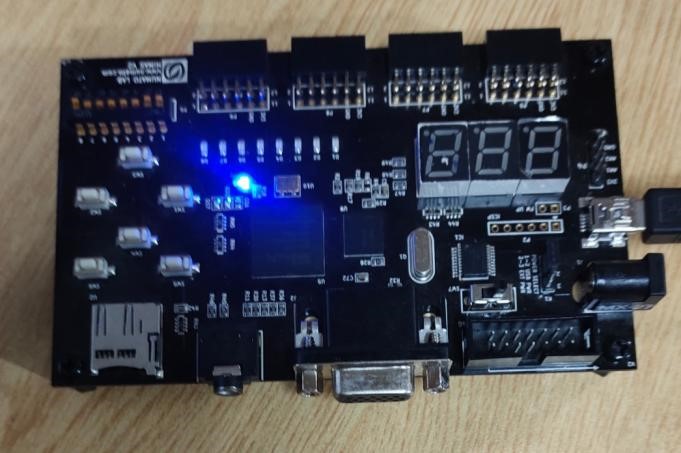
**TASK 1:**

Implement 4 bit Ring Counter

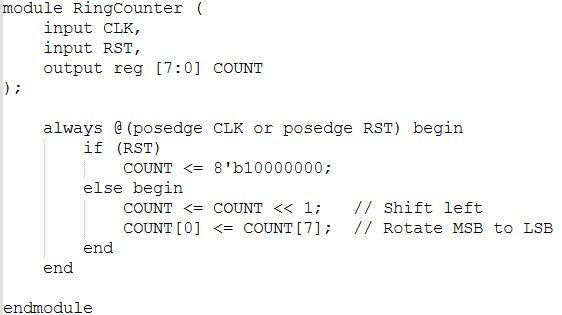
**CODE:**



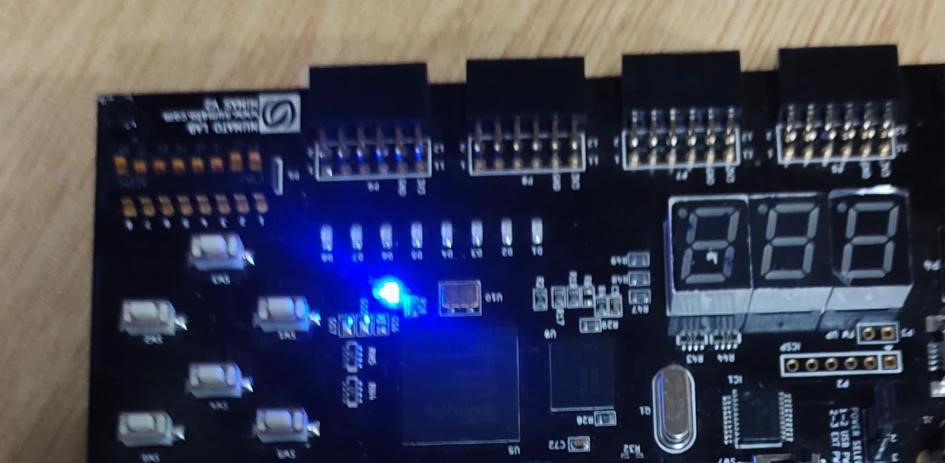
**OUTPUT:**



**TASK 2:** Implement 8-bit Ring Counter **CODE:**



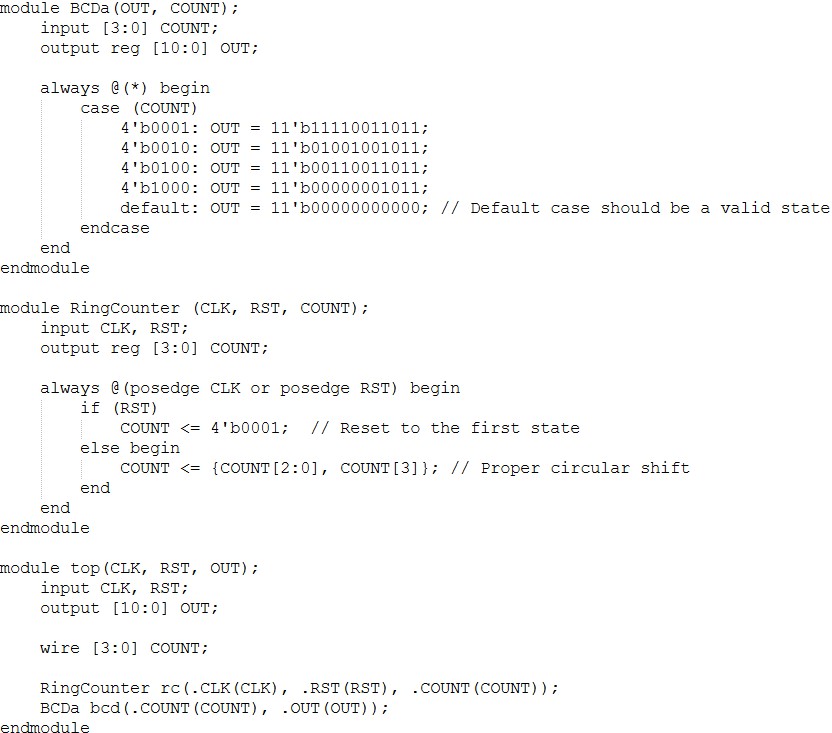
**OUTPUT:**



**TASK 3:**

For 4 bit Ring counter display the count in the seven segment display

**CODE:**



**OUTPUT:**

